REMARKS

Claims 3, 5-8, 11, 14-17, and 22-31 are currently pending. Reexamination and reconsideration of the application are respectfully requested.

REJECTION OF CLAIMS 3, 5, 11, 14, and 22-30 UNDER 35 U.S.C. 102

Claims 3, 5, 11, 14, and 22-30 are rejected under 35 U.S.C. 102(c) for the reasons set forth on pages 3-4 of the Action. Specifically, claims 3, 5, 11, 14, and 22-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Yonemoto et al. (US Pat. No. 6,166,769), which is hereinafter referred to as "Yonemoto" or as "the Yonemoto reference."

The rejections under 35 U.S.C. 102(e) are respectfully traversed, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth herein below.

The Federal Circuit has ruled, "Under 35 U.S.C. §102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. . . . In addition, the prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public." Akzo N.V. v. United States Int'l Trade Comm'n, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). [emphasis added.]

Furthermore, the Federal Circuit has held, "Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). [emphasis added.]

It is respectfully submitted that the Yonemoto reference fails to teach or suggest each and every element of the system as claimed. Specifically, the Yonemoto reference fails to teach

or suggest, the first sampling circuit as claimed. For example, the Action cites elements 38 and 38' of Yonemoto et al. taken together to teach the first sampling circuit as claimed. However, elements 38 and 38', whether alone, or in combination fail to fairly teach or suggest the first sampling circuit, the first switch, and the specific limitations regarding the coupling between the first sampling circuit and the first switch as required by independent claims 22 and 23.

Applicant appreciates the labeling of prior art FIG. 4 to indicate how Examiner is applying the prior art to the claimed invention. However, combining circuit 38 and 38' to teach a first sampling circuit as claimed appears to contradict the clear teaching of Yonemoto et al. Col. 7, lines 15-20 of Yonemoto et al. states, "The first operation switches 37, the first load capacitance elements 38, and the first horizontal switches 39 jointly make up a first signal holding circuit 51 for holding signals of the pixel MOS transistors before the pixels are reset." In other words, Yonemoto et al. considers elements 37, 38 and 39 to comprise a first signal holding circuit 51. Similarly, col. 7, lines 18-22 of Yonemoto et al. states, "The second operation switches 37', the second load capacitance elements 38', and the second horizontal switches 39' jointly make up a second signal holding circuit 52 for holding signals of the pixel MOS transistors after the pixels are reset."

Consequently, it is a strained interpretation to combine elements 38 and 38' to form a single holding circuit when the Yonemoto reference itself clearly teaches against such an interpretation by describing two separate holding circuits 51, 52, each with the components as described above.

Moreover, Yonemoto et al. fails to teach or suggest, "wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column," as claimed.

The first hold circuit 51 of Yonemoto is for "holding signals of the pixel MOS transistors before the pixels are reset." (col. 7, lines 17-18). The second hold circuit 52 of Yonemoto is for "holding signals of the pixel MOS transistors after the pixels are reset." (col. 7, lines 21-22). Neither of these circuits 51, 52 samples two signals (e.g., a light signal and a reset signal) as claimed.

In other words, Yonemoto utilizes a first capacitor 38 for sampling the signal value before pixel reset and a second, separate capacitor 38' for sampling the signal value after pixel reset. Moreover, Yonemoto clearly indicates that two sample and hold circuits (a first signal holding circuit 51 and a second signal holding circuit 52) are utilized per column in its solid-state imaging device. In sharp contrast, the claimed invention employs for each column a single sampling circuit that samples both a light signal and a reset signal from a photocell as claimed.

The dependent claims incorporate all the limitations of independent claims 22 and 23, respectively. In this regard, the dependent claims also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited reference.

In view of the foregoing, it is respectfully submitted that Yonemoto reference, whether alone or in combination, fails to teach or suggest the sequential readout circuit and system as claimed.

REJECTION OF CLAIMS 6, 7, 8, 15, 16 and 17 UNDER 35 U.S.C. 103(a)

Claims 6, 7, 15, and 16 are rejected under 35 U.S.C. 103 on pages 3 and 4 of the Action as being unpatentable over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Simerly et al. (U.S. Pat. No. 5,982,424). Also, claims 8 and 17 are rejected under 35 U.S.C. 103 on page 4 of

the Action as being unpatentable over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Krymski et al. (U.S. Pat. No. 6,222,175).

The Action states that Yonemoto does not disclose level shifting circuit or gain manipulation circuit as claimed. However, the Action cites Simerly et al. (col. 7, lines 35-47) for teaching "level shifting and gain manipulation in a similar system." The Action further states "it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide such a configuration in the apparatus of Yonemoto to improve detection."

The rejections under 35 U.S.C. 103 are respectfully traversed, and reconsideration and reexamination of the application are respectfully requested for the reasons set forth hereinbelow. The combination of the readout circuit of Yonemoto with "level shifting and gain manipulation," purportedly taught by Simerly et al., is contested as improper for the reasons advanced in responses to previous Actions. However, even if this combination were proper, which is not conceded, the resulting combination would still fail to teach or suggest the claimed invention.

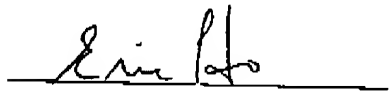
It is respectfully submitted that the combination of Yonemoto and Simerly (or Yonemoto and Krymski) fails to teach or suggest the invention as claimed for the same reasons as advanced previously. Simerly and Krymski do not cure the deficiencies of Yonemoto. Specifically, it is noted that the Yonemoto reference, whether alone or in combination with Simerly et al. or Krymski, fails to teach or suggest inter alia the following claim limitations: "wherein the first sampling circuit samples a light signal and a reset signal from each photocell

in the first column," and the specific coupling of the first sampling circuit with the first switch as recited in amended claims 22 and 23.

It appears that the current patent application has been improperly used as a basis for the motivation to combine or modify the components selected from Yonemoto, Simerly or Krymski to arrive at the claimed invention. Stated differently, the proposed combination of the cited references appear to be based on hindsight since the cited references do not teach or suggest a motivation to combine the respective elements of each reference in the manner proposed by the Action. Accordingly, it is respectfully requested that the rejection of claims 6, 7, 8, 15, 16 and 17 under 35 U.S.C. 103(a) be withdrawn.

For all the reasons advanced above, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the pending claims are requested, and allowance is earnestly solicited at an early date. The Examiner is invited to telephone the undersigned if the Examiner has any suggestions, thoughts or comments, which might expedite the prosecution of this case.

Respectfully submitted,



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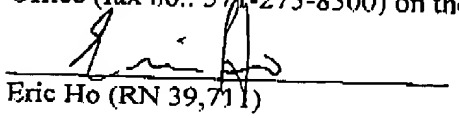

Eric Ho (RN 39,711) March 8, 2006
(Date)